

NEUB CSE 222 LAB 2: More into Logic Gates

North East University Bangladesh

Department of CSE

Course no: CSE 222

Experiment no: 02

Experiment Name: More into Logic Gates

CAUTIONS:

1. Don't switch on the supply of the circuit until you have verified the circuit carefully
2. Take readings of apparatus carefully
3. Take care of any bare circuit elements in energized condition
4. Never try to touch bare live wires

Objective

The objective of this experiment is to experiment more with the logic gate ICs and Create multi input logic gates using only 2 input gates.

Theory

Multiple 2 input and gates can be combined to create multi input gates. Also different gate can be implemented by combining multiple gates.

Apparatus Needed

- Trainer Board (Bread board)
- Logic Gate ICs (List in next section)
- Connecting wires
- LEDs
- Push Buttons / DIP switch

Logic Gate ICs

IC number	IC name
7404	Hex inverter
7408	Quad 2 input AND gate
7432	Quad 2 input OR gate
7400	Quad 2 input NAND gate
7402	Quad 2 input NOR gate
7486	Quad 2 input XOR gate

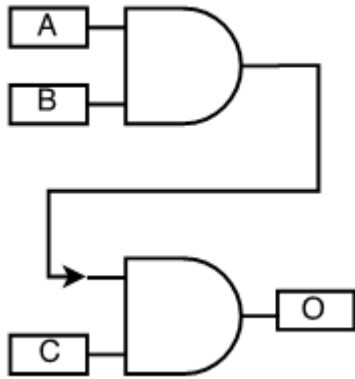
Procedure

1. Place the IC in the in the breadboard
2. Connect VCC and Ground to the respective pins of IC
3. Connect the inputs switches provided in the IC trainer kit
4. Connect all the internal connections
5. Connect the output of the ICs to LEDs
6. Apply various combinations of inputs according to the tables of result section
7. Observe and write the output of the LED in the corresponding table in result section.
8. Repeat for all the circuits in the result section.

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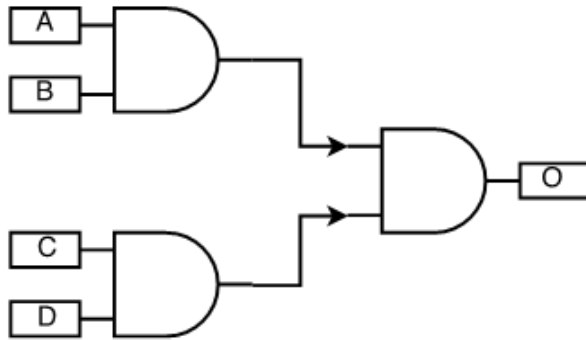
Result

1.



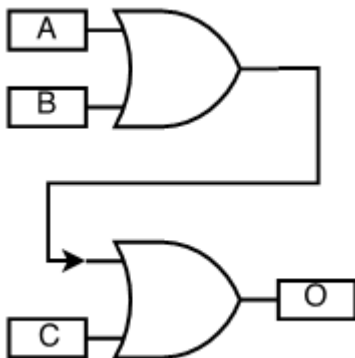
A	B	C	O
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

2.



A	B	C	D	O
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

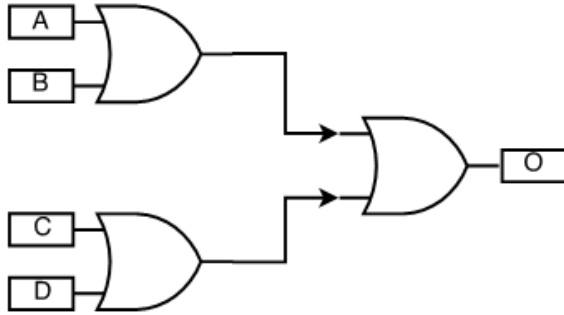
3.



A	B	C	O
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

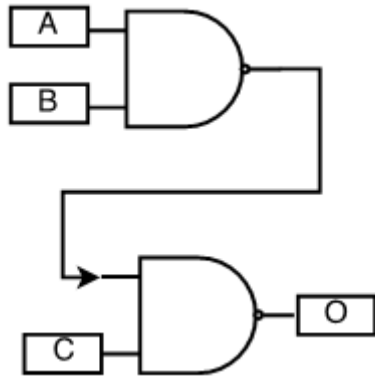
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4.



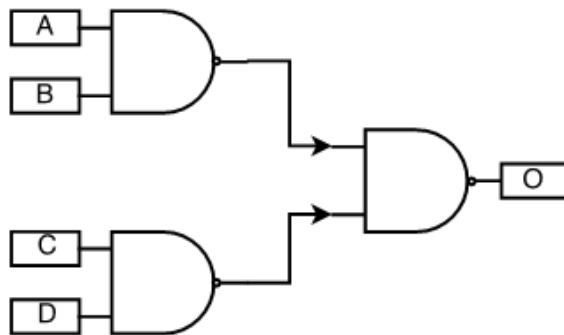
A	B	C	D	O
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

5.



A	B	C	O
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

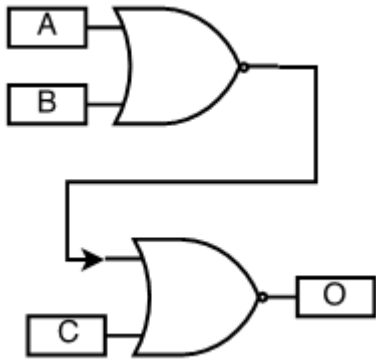
6.



A	B	C	D	O
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

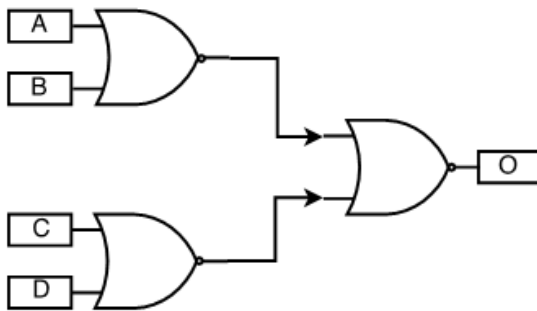
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7.



A	B	C	O
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

8.



A	B	C	D	O
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

Report

1. Carefully fill all the data for table 1 to 8.
2. Comment on the learning from this LAB